

1. General description

Planar passivated high commutation three quadrant triac in an IITO220 internally insulated plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series B" triac will commutate the full RMS current at the maximum rated junction temperature without the aid of a snubber. This device has high T_j operating capability and an internally isolated mounting base.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High junction operating temperature capability ($T_{j(max)} = 150^\circ\text{C}$)
- High surge capability
- Isolated mounting base with 2500 V (RMS) isolation
- Least sensitive gate for highest noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- Electronic thermostats (heating and cooling)
- High power motor controls
- Rectifier-fed DC inductive loads e.g. DC motors and solenoids

4. Quick reference data

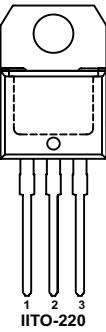
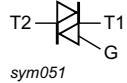
Table 1. Quick reference data

Symbol	Parameter	Conditions	Values	Unit
Absolute maximum rating				
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	square-wave pulse; $T_{mb} \leq 116^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	12	A
I_{TSM}	non-repetitive peak forward current	full sine wave; $t_p = 20\text{ ms}$; $T_{j(init)} = 25^\circ\text{C}$; Fig. 4 ; Fig. 5	140	A
		full sine wave; $t_p = 16.7\text{ ms}$; $T_{j(init)} = 25^\circ\text{C}$	153	A
T_j	junction temperature		150	$^\circ\text{C}$

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+ T _j = 25 °C; Fig. 7		2	-	50	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G- T _j = 25 °C; Fig. 7		2	-	50	mA
		V _D = 12 V; I _T = 0.1 A; T2- G- T _j = 25 °C; Fig. 7		2	-	50	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9		-	-	60	mA
V _T	on-state voltage	I _T = 18 A; T _j = 25 °C; Fig. 10		-	1.3	1.5	V
Dynamic characteristics							
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit		1000	-	-	V/μs
		V _{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit		600	-	-	V/μs
dI _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 20 V/μs; gate open circuit; snubberless condition		20	-	-	A/ms
		V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 20 V/μs; gate open circuit; snubberless condition		8	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	n.c	mounting base; isolated	 ITO-220	 sym051

6. Ordering information

Table 3. Ordering information

Type number	Package name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BTA412Y-800B	ITO220	BTA412Y-800B,127	Tube	50	ITO220E	15-Dec-2020

7. Marking

Table 4. Marking codes

Type number	Marking codes
BTA412Y-800B	BTA412Y-800B

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 116^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	12	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $t_p = 20 \text{ ms}$; $T_{j(\text{init})} = 25^{\circ}\text{C}$; Fig. 4 ; Fig. 5	140	A
		full sine wave; $t_p = 16.7 \text{ ms}$; $T_{j(\text{init})} = 25^{\circ}\text{C}$	153	A
I^2t	I^2t for fusing	$t_p = 10\text{ms}$; sine wave	98	A^2/s
dI_T/dt	rate of rise of on-state current	$I_G = 100\text{mA}$	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		2	A
P_{GM}	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
T_{stg}	storage temperature		-40 to 150	$^{\circ}\text{C}$
T_j	junction temperature		150	$^{\circ}\text{C}$

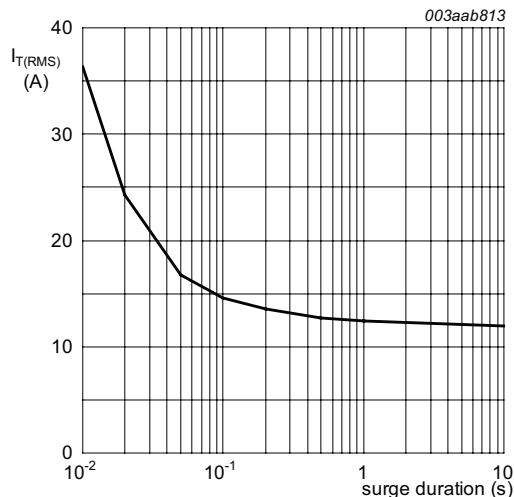


Fig. 1. RMS on-state current as a function of surge duration; maximum values

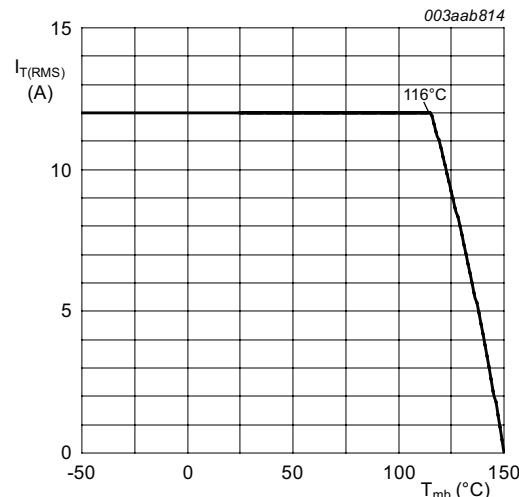
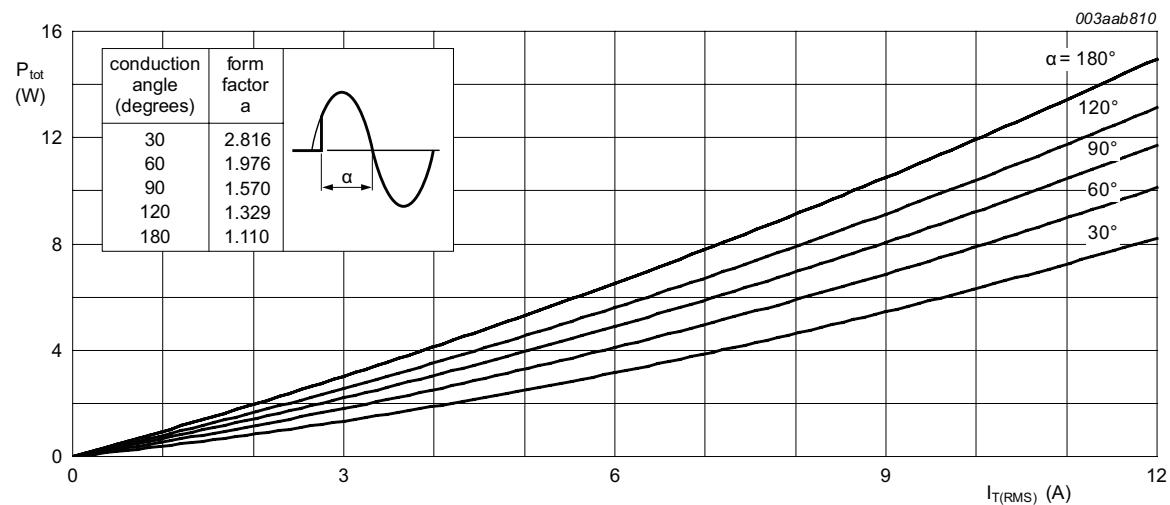


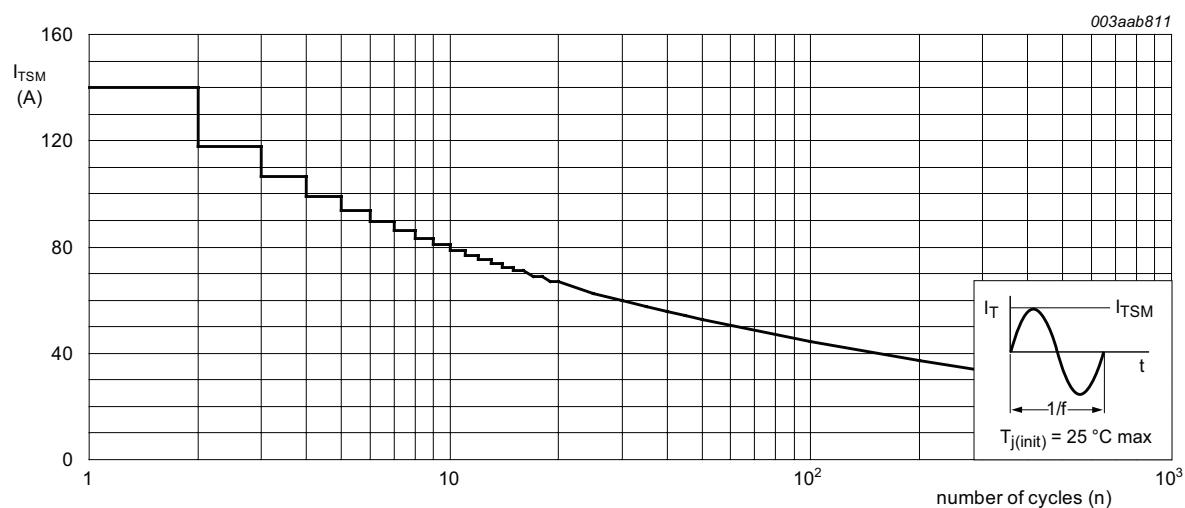
Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



α = conduction angle

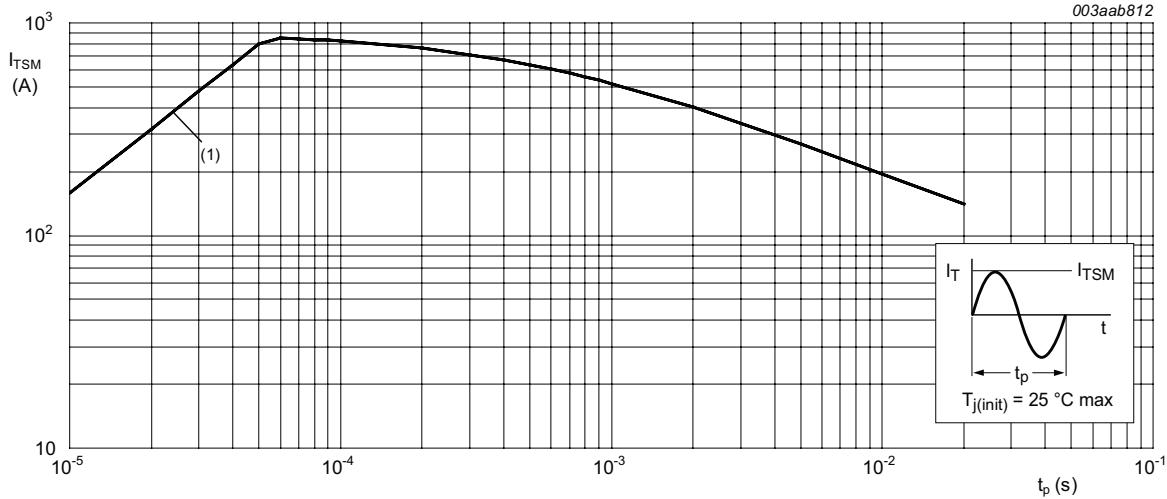
a = form factor = $I_{T(\text{RMS})} / I_{T(\text{AV})}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



$f = 50 \text{ Hz}$

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20 \text{ ms}$;
(1) dI_t/dt limit

Fig. 5. Total power dissipation as a function of RMS on-state current; maximum values

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 6		-	-	2.1	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient free air	in free air		-	60	-	K/W

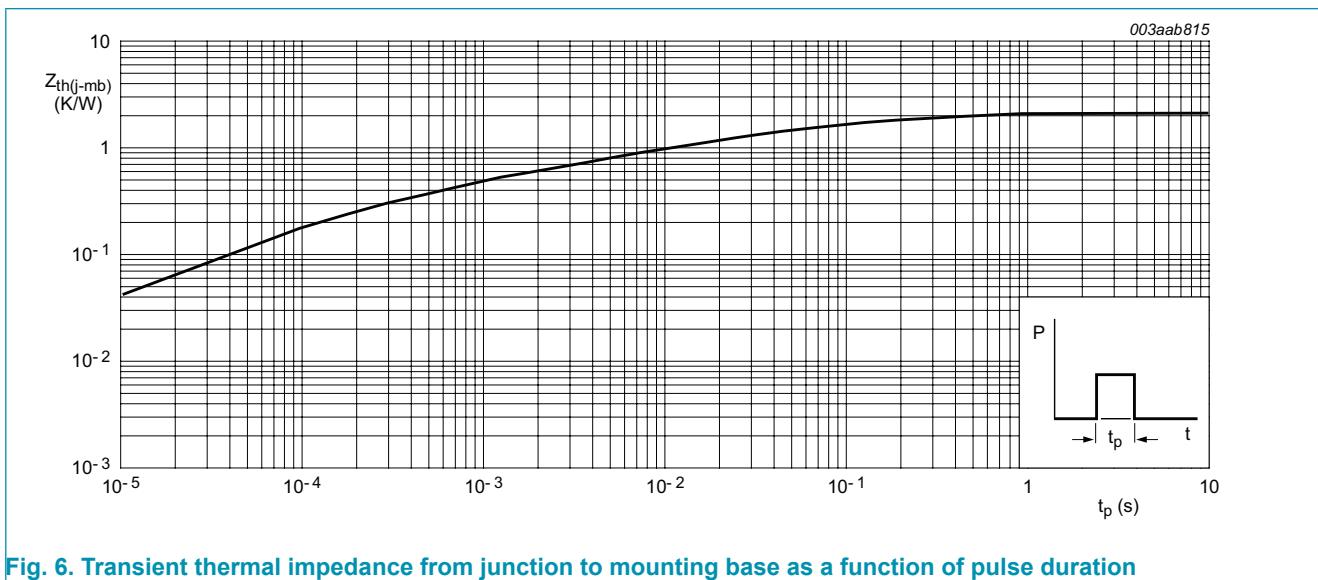


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	$50 \text{ Hz} \leq f \leq 60 \text{ Hz}$; $\text{RH} \leq 65\%$; from all pins to external heatsink; sinusoidal waveform; clean and dust free		-	-	2500	V
C_{isol}	isolation capacitance	from cathode to external heatsink		-	10	-	pF

11. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_2+ \text{ G}+; T_j = 25^\circ\text{C};$ Fig. 7		2	-	50	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_2+ \text{ G}-; T_j = 25^\circ\text{C};$ Fig. 7		2	-	50	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_2- \text{ G}-; T_j = 25^\circ\text{C};$ Fig. 7		2	-	50	mA
I_L	latching current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_2+ \text{ G}+; T_j = 25^\circ\text{C};$ Fig. 8		-	-	60	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_2+ \text{ G}-; T_j = 25^\circ\text{C};$ Fig. 8		-	-	90	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_2- \text{ G}-; T_j = 25^\circ\text{C};$ Fig. 8		-	-	60	mA
I_H	holding current	$V_D = 12 \text{ V}; T_j = 25^\circ\text{C};$ Fig. 9		-	-	60	mA
V_T	on-state voltage	$I_T = 18 \text{ A}; T_j = 25^\circ\text{C};$ Fig. 10		-	1.3	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25^\circ\text{C};$ Fig. 11		-	0.8	1	V
		$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; T_j = 150^\circ\text{C}$		0.25	0.4	-	V
I_D	off-state current	$V_D = 800 \text{ V}; T_j = 125^\circ\text{C}$		-	0.1	0.5	μA
		$V_D = 800 \text{ V}; T_j = 150^\circ\text{C}$		-	0.4	2	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536 \text{ V}; T_j = 125^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM});$ exponential waveform; gate open circuit		1000	-	-	V/ μs
		$V_{DM} = 536 \text{ V}; T_j = 150^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM});$ exponential waveform; gate open circuit		600	-	-	V/ μs
dl_{com}/dt	rate of change of commutating current	$V_D = 400 \text{ V}; T_j = 125^\circ\text{C}; I_{T(RMS)} = 12 \text{ A}; dV_{com}/dt = 20 \text{ V}/\mu\text{s};$ gate open circuit; snubberless condition		20	-	-	A/ms
		$V_D = 400 \text{ V}; T_j = 150^\circ\text{C}; I_{T(RMS)} = 12 \text{ A}; dV_{com}/dt = 20 \text{ V}/\mu\text{s};$ gate open circuit; snubberless condition		8	-	-	A/ms

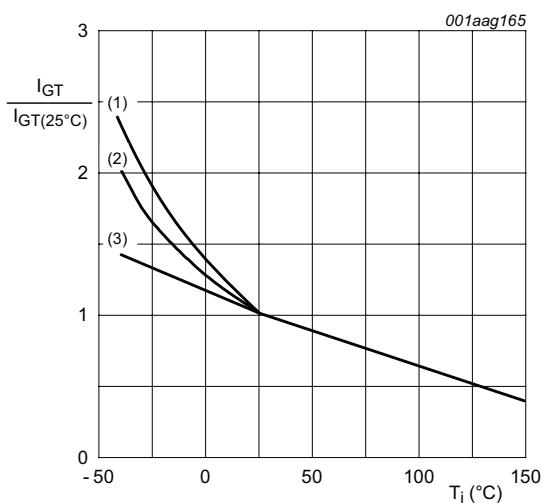


Fig. 7. Normalized gate trigger current as a function of junction temperature

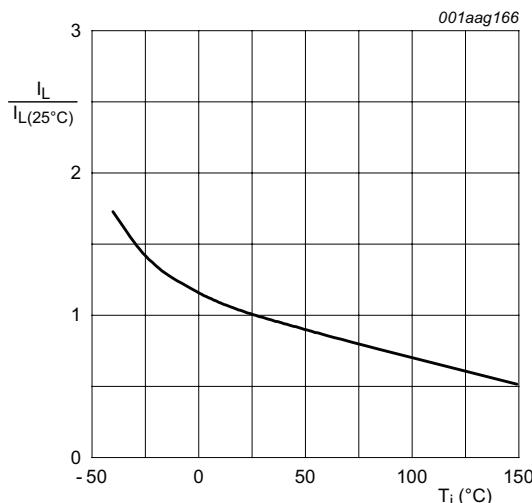


Fig. 8. Normalized latching current as a function of junction temperature

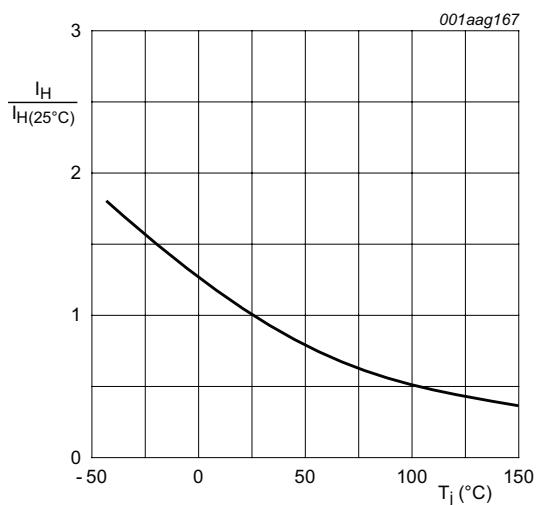


Fig. 9. Normalized holding current as a function of junction temperature

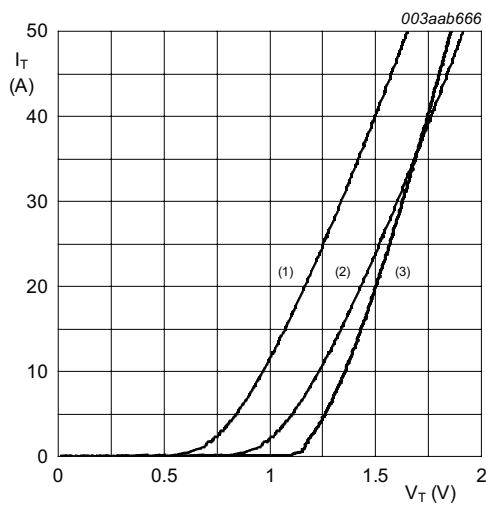


Fig. 10. On-state current as a function of on-state voltage

$V_o = 1.024 \text{ V}$; $R_s = 0.021 \Omega$
 (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
 (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

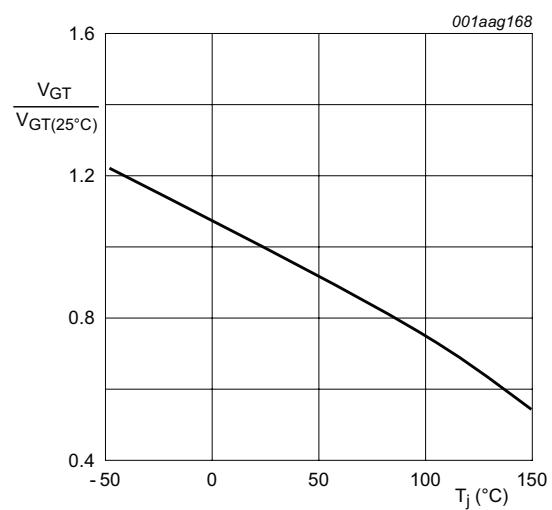
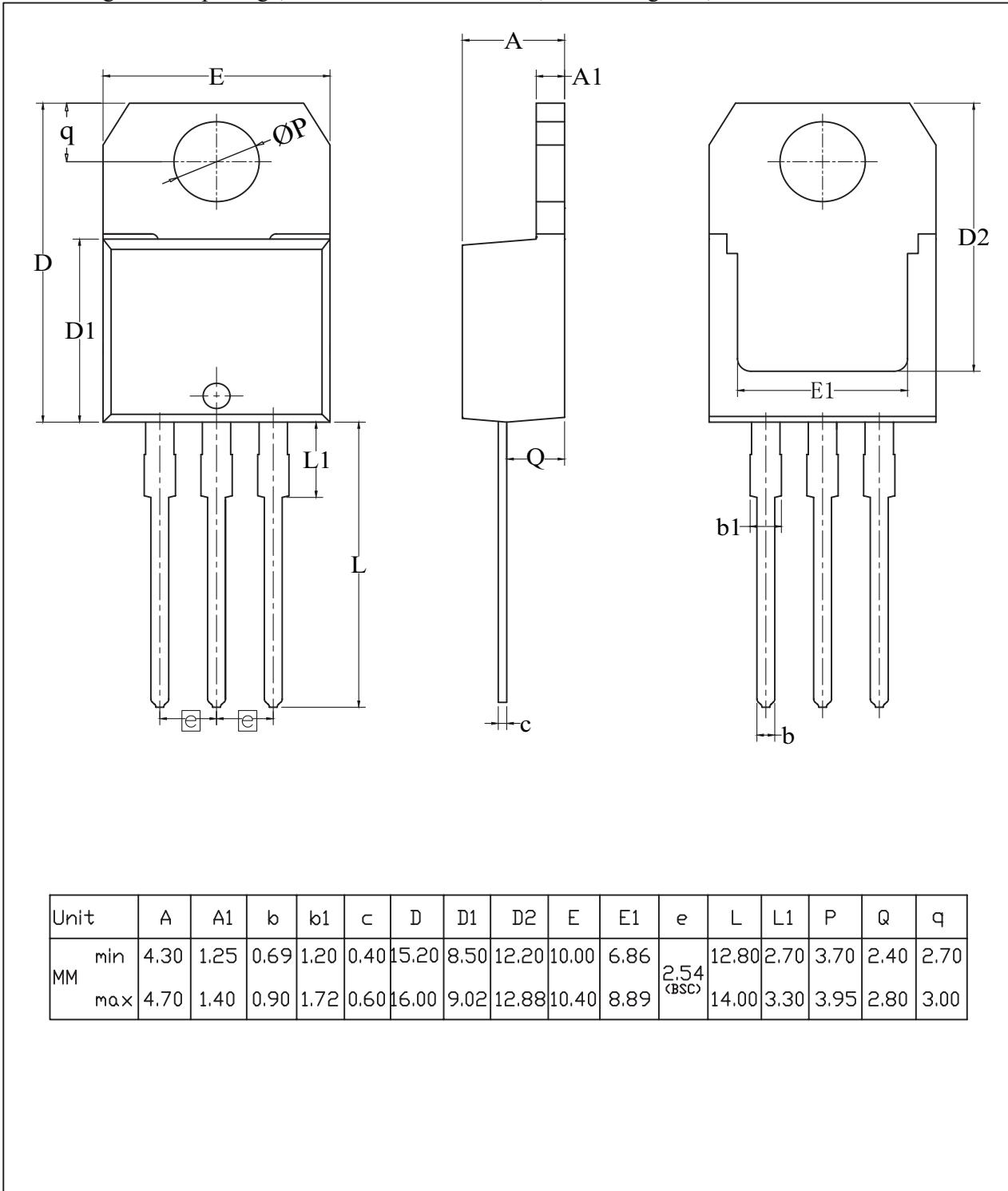


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

12. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 leads TO-220 IITO220



IMPORTANT NOTICE – PLEASE READ CAREFULLY

SZGKTMicroelectronics NV and its subsidiaries reserve the right to make changes, corrections, enhancements, modifications, and improvements to SZGKT.