

GENERAL DESCRIPTION

Planar passivated thyristors in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

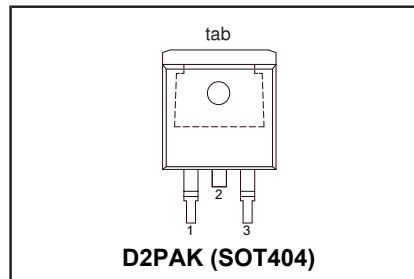
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
V_{DRM} , V_{RRM}	BT152B- Repetitive peak off-state voltages	400R 450	600R 650	800R 800	V
$I_{T(AV)}$	Average on-state current	13	13	13	A
$I_{T(RMS)}$	RMS on-state current	20	20	20	A
I_{TSM}	Non-repetitive peak on-state current	200	200	200	A

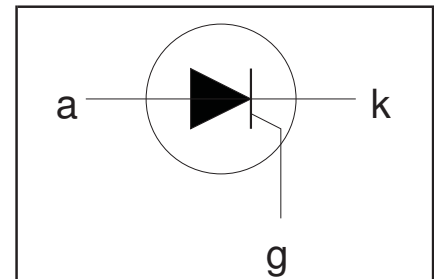
PINNING - SOT404

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
mb	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-400R 450 ¹	-600R 650 ¹	-800R 800	
V_{DRM}	Repetitive peak off-state voltages		-				V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 103\text{ }^\circ\text{C}$	-	13			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	20			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ }^\circ\text{C}$ prior to surge	-	200			A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	200			A
di_T/dt	Repetitive rate of rise of on-state current after triggering	$t = 8.3\text{ ms}$	-	220			A
		$t = 10\text{ ms}$	-	200			A ² s
		$I_{TM} = 50\text{ A}; I_G = 0.2\text{ A}; di_G/dt = 0.2\text{ A}/\mu\text{s}$	-	200			A/ μs
I_{GM}	Peak gate current		-	5			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	20			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			$^\circ\text{C}$
T_j	Operating junction temperature		-	125			$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	minimum footprint, FR4 board	-	-	1.1	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	3	32	mA
I_L	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	25	80	mA
I_H	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	15	60	mA
V_T	On-state voltage	$I_T = 40\text{ A}$	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.6	1.5	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}; I_T = 0.1\text{ A}; T_j = 125\text{ °C}$ $V_D = V_{DRM(max)}; V_R = V_{RRM(max)}; T_j = 125\text{ °C}$	0.25	0.4	-	V
			-	0.2	1.0	mA

DYNAMIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ exponential waveform gate open circuit	200	300	-	V/ μ s
t_{gt}	Gate controlled turn-on time	$V_D = V_{DRM(max)}; I_G = 0.1\text{ A}; dI_G/dt = 5\text{ A}/\mu\text{s};$ $I_{TM} = 40\text{ A}$	-	2	-	μ s
t_q	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ $I_{TM} = 50\text{ A}; V_R = 25\text{ V}; dI_{TM}/dt = 30\text{ A}/\mu\text{s};$ $dV_D/dt = 50\text{ V}/\mu\text{s}; R_{GK} = 100\ \Omega$	-	70	-	μ s

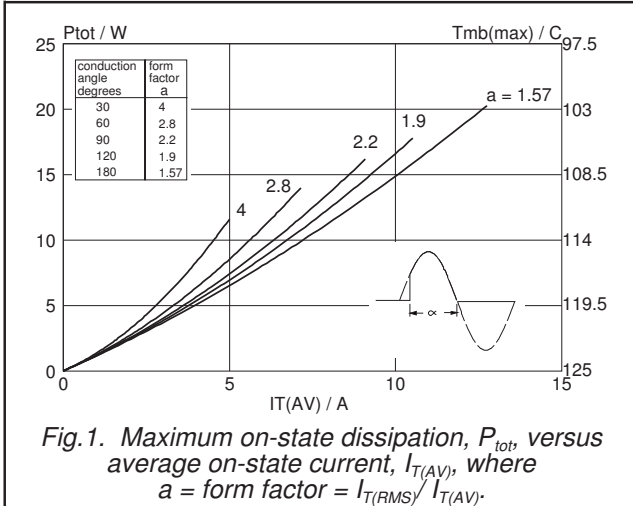


Fig. 1. Maximum on-state dissipation, P_{tot} , versus average on-state current, $I_{T(AV)}$, where $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$.

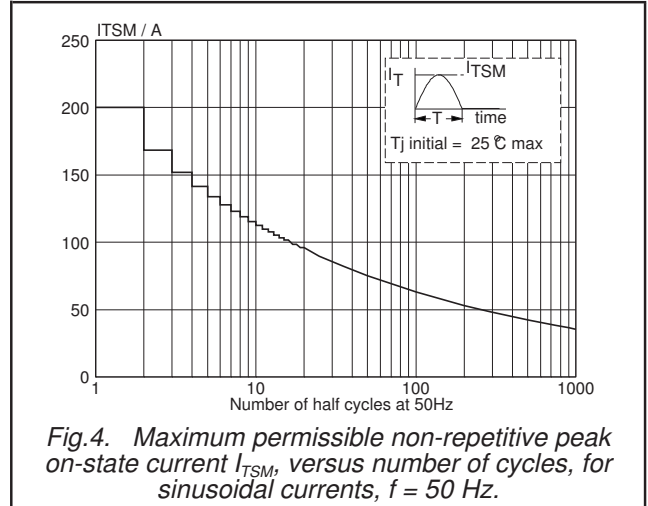


Fig. 4. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50 \text{ Hz}$.

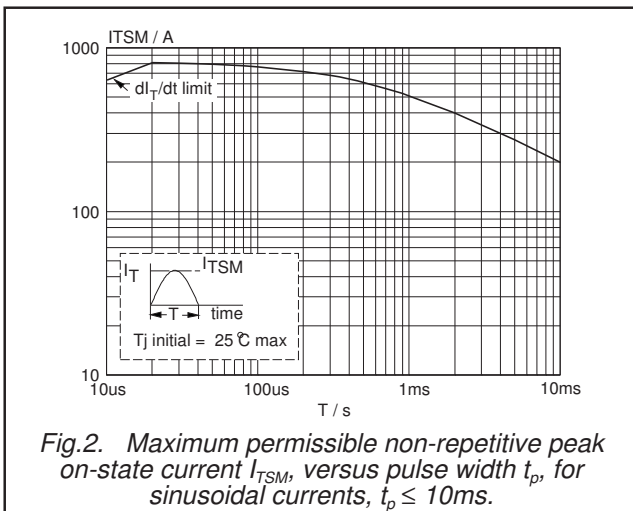


Fig. 2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10 \text{ ms}$.

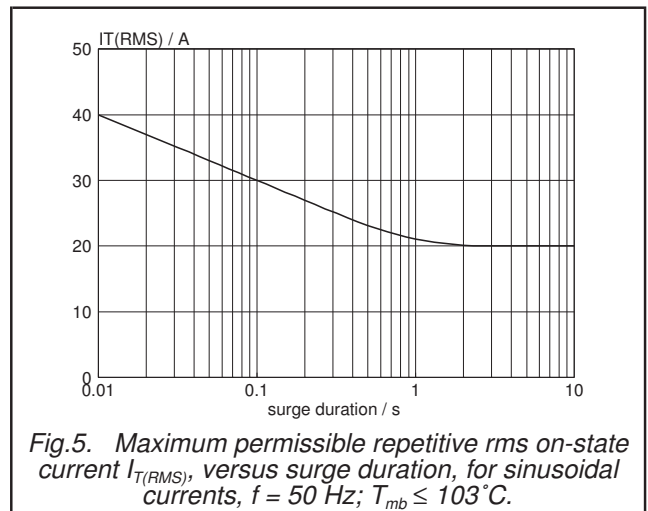


Fig. 5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50 \text{ Hz}$; $T_{mb} \leq 103^\circ\text{C}$.

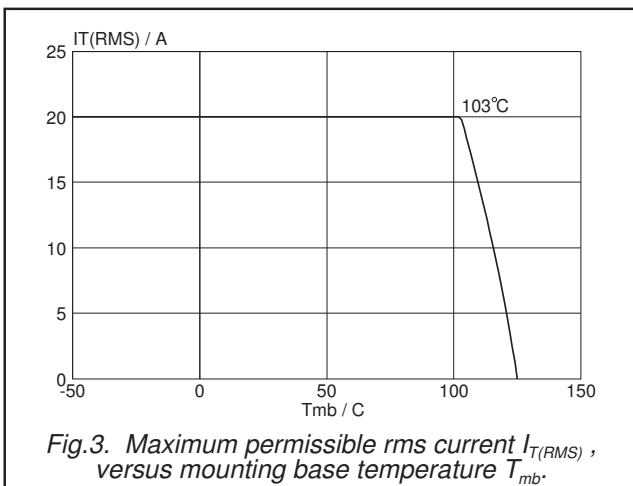


Fig. 3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb} .

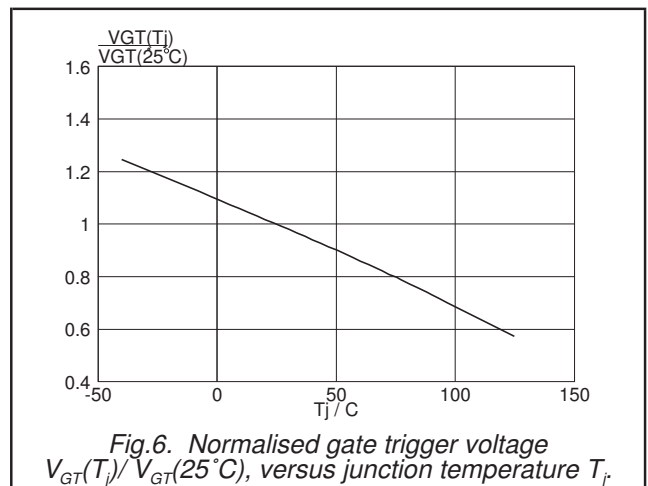
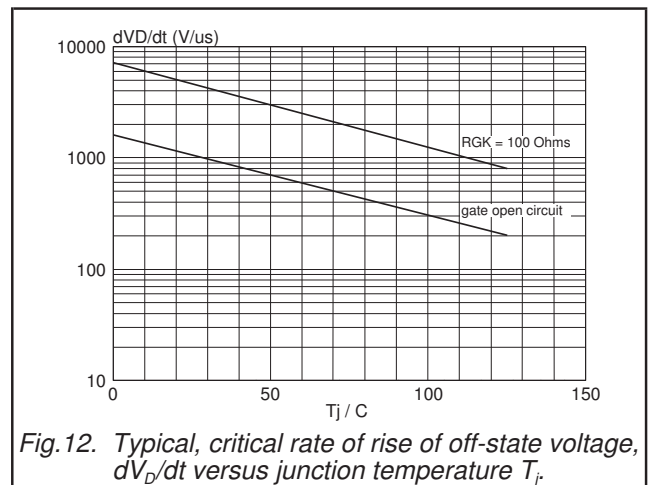
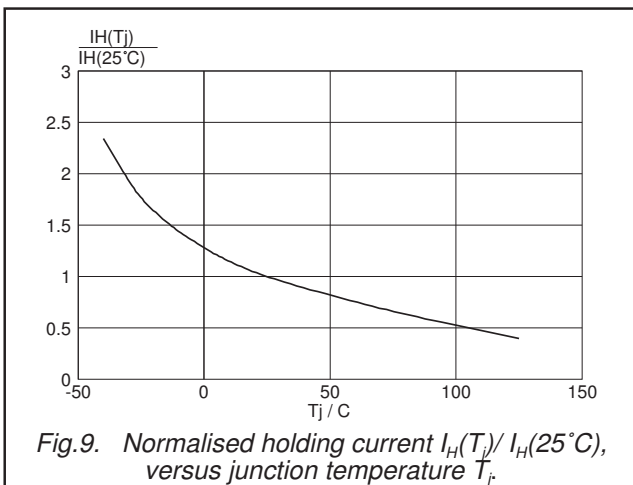
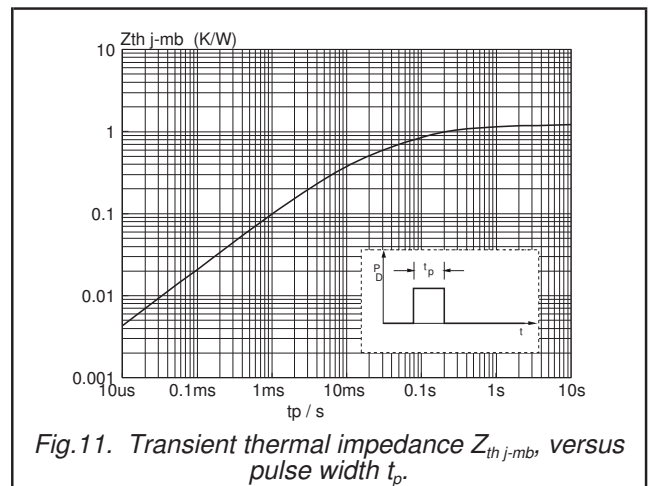
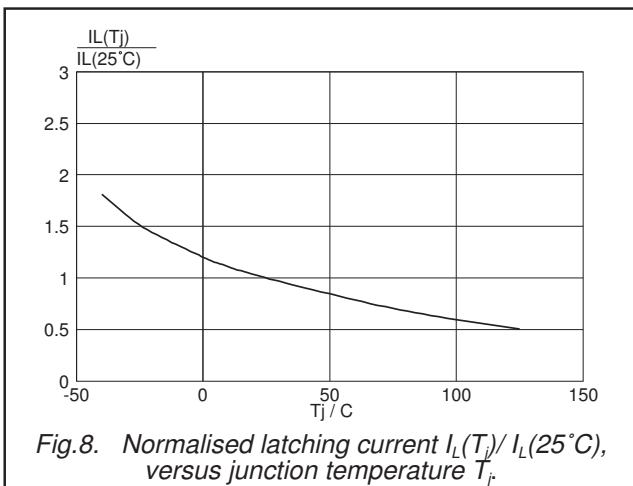
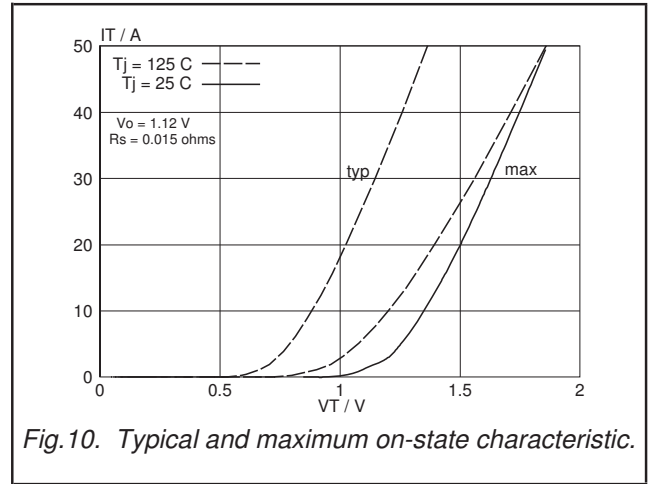
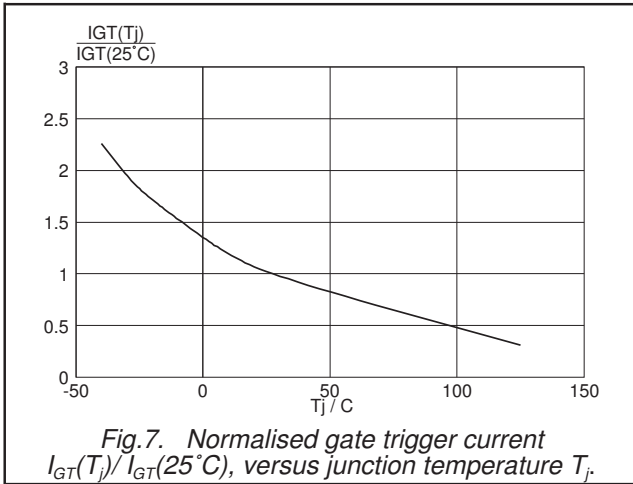


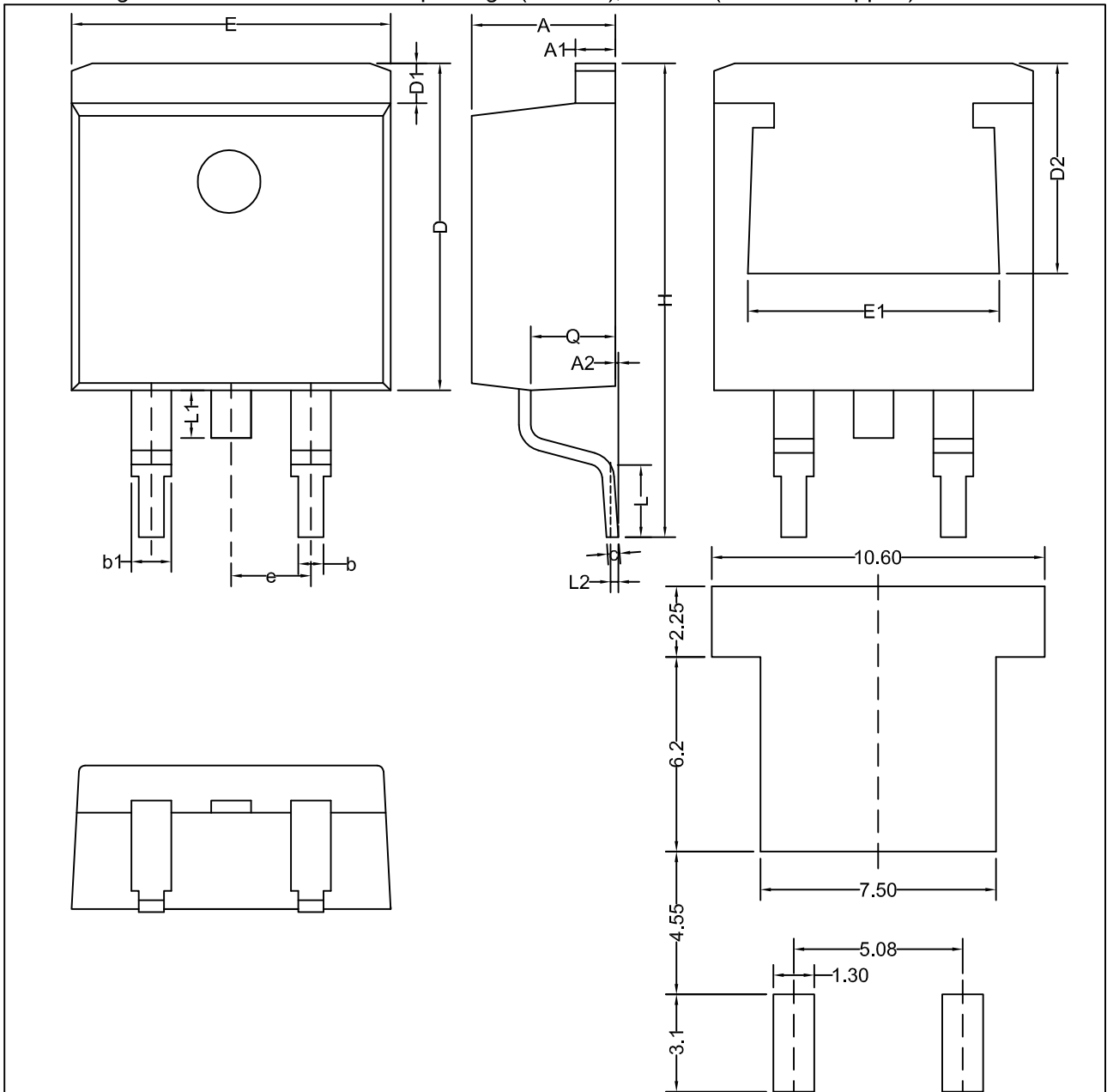
Fig. 6. Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .



MECHANICAL DATA

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

TO263



Recommended Footprint

	A	A1	A2	b	b1	c	D	D1	D2	e	E	E1	H	L	L1	L2	Q
min	4.10	1.22	0.00	0.60	1.05	0.34	---	1.20	6.60		9.70	7.80	14.80	2.10	---		2.20
max	4.70	1.40	0.25	0.90	1.45	0.64	11.00	1.60	---	2.54 (BSC)	10.30	---	15.80	2.90	1.75	0.25 (BSC.)	2.79

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